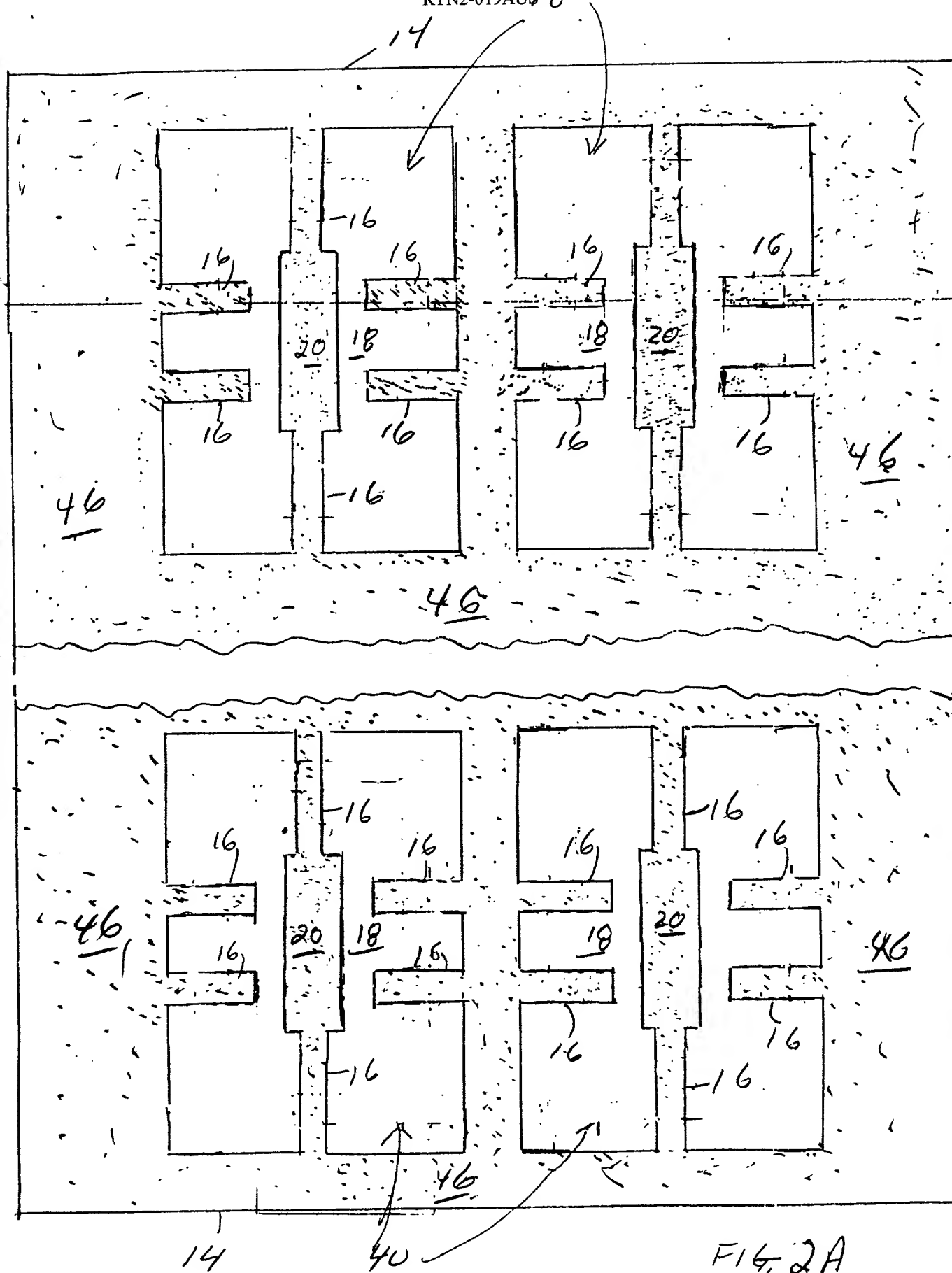
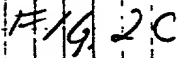
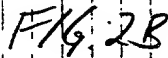


FIG. 2A





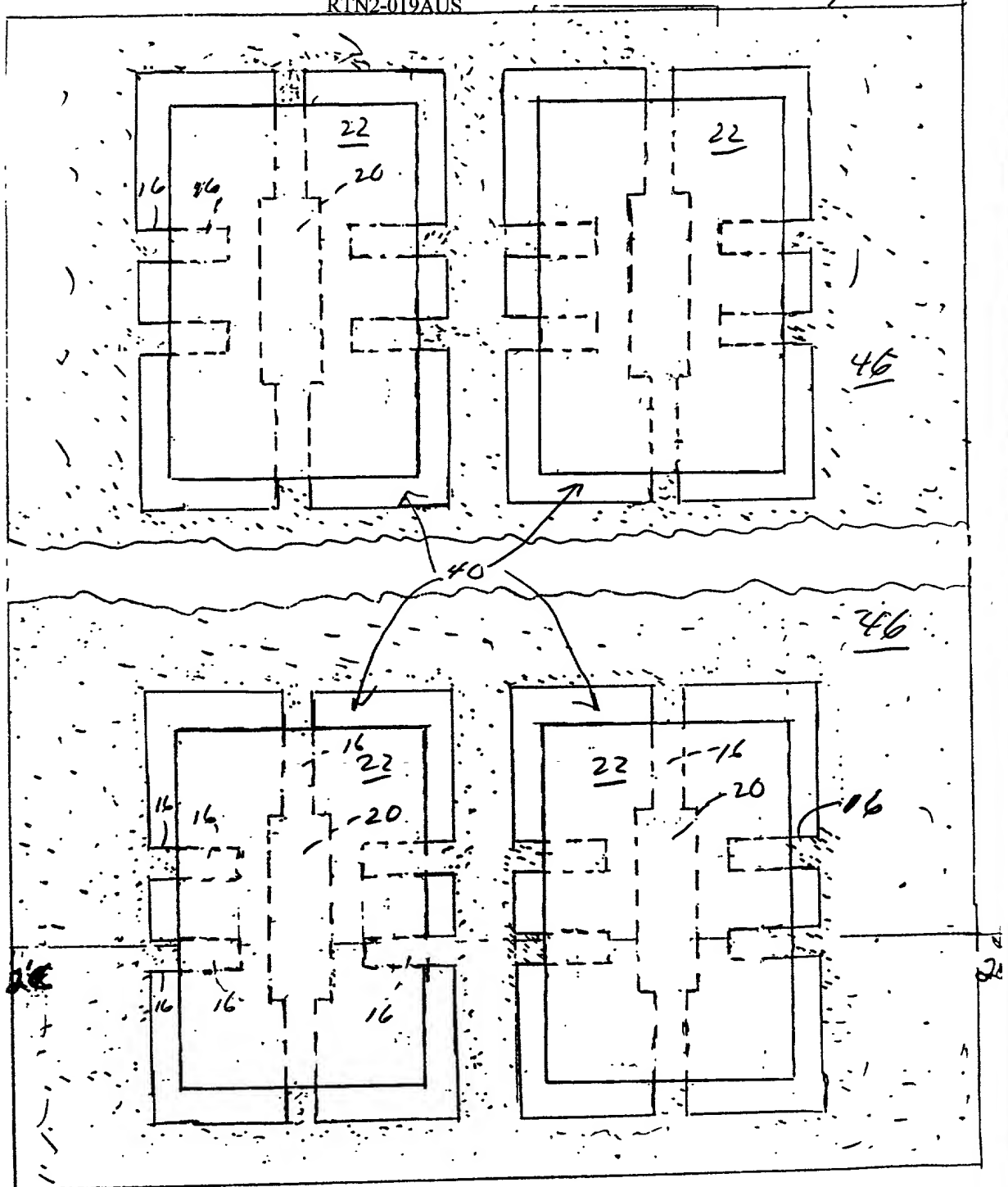
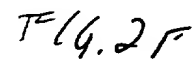
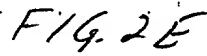


FIG. 2.D

TOP SECRET



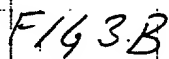
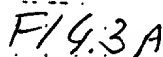




FIG 4A

Integrated Circuit Chip Package

Edward C. Douglas

RTN2-019AUS

FIG. 4B

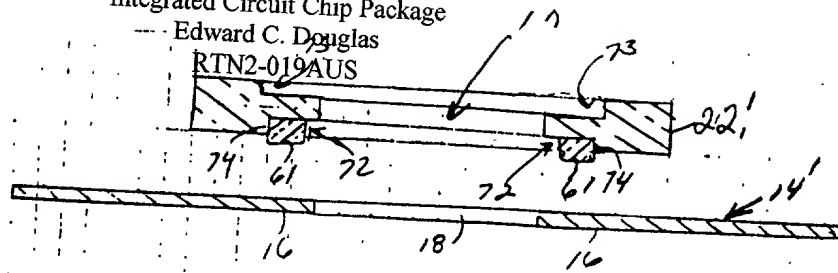


FIG. 4C

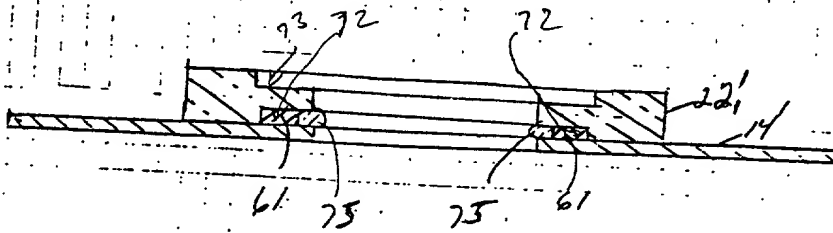


FIG. 4D

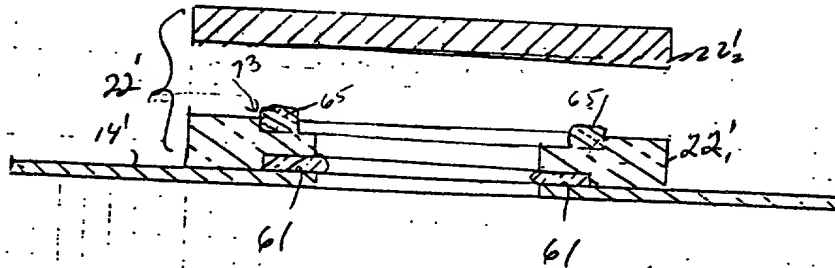


FIG. 4E

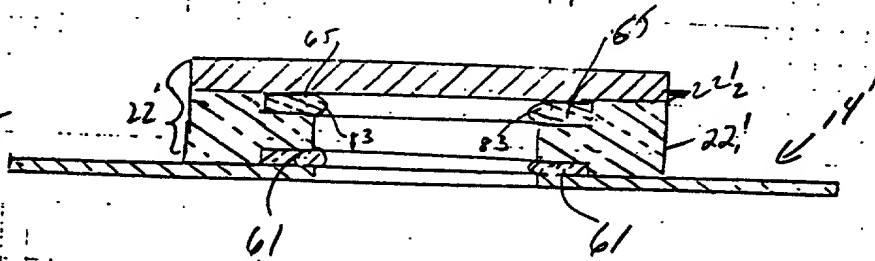


FIG. 4F

